PCI Hot Plug Controller

The HIP1011 is the PCI Hot Plug voltage bus control IC for use in modern computer systems that facilitates hot plugging of adapter cards into and out of an active or passive back plane. Along with discrete power MOSFETs and a few passive components, the HIP1011 creates a small and simple yet complete power control solution. Four independent supplies are controlled, +5V, +3.3V, +12V, and -12V. The +12V and -12V switches are integrated. For the +5V and +3.3V supplies, overcurrent protection is provided by sensing the voltage across external current-sense resistors. For the +12V and -12V supplies, overcurrent protection is provided internally. In addition, an on-chip reference is used to monitor the +5V, +3.3V and +12V outputs for undervoltage conditions. The PWRON input controls the state of the switches. During an overcurrent condition on any output, or an undervoltage condition on the +5V, +3.3V or +12V outputs, all MOSFETs are immediately latched-off and a LOW (0V) is asserted on the FLTN output. The FLTN latch is cleared when the PWRON input is toggled low again. During initial power-up of the main V_{CC} supply (+12V), the PWRON input is inhibited from turning on the switches, and the latch is held in the Reset state until the V_{CC} input is greater than 10V.

User programmability of the overcurrent threshold and turn-on slew rate is provided. A resistor connected to the OCSET pin programs the overcurrent threshold. Capacitors connected to the gate pins set the turn-on rate. Also, a capacitor may be added to the FLTN pin to provide noise immunity.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP1011CB	0 to 70	16 Ld SOIC	M16.15
HIP1011CB-T	0 to 70	Tape and Reel	
HIP1011CBZA (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
HIP1011CBZA-T (Note)	0 to 70	Tape and Reel (Pb-free)	
HIP1011EVAL1	Evaluation Platform		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

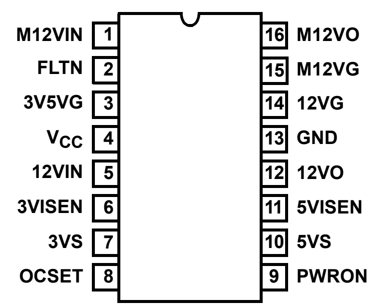
- Controls Distribution of Four Supplies: +5V, +3.3V, +12V, and -12V
- Internal MOSFET Switches for +12V and -12V Outputs
- Microprocessor Interface for On/Off Control and Fault Reporting
- Adjustable Overcurrent Protection for All Supplies
- Provides Fault Isolation
- Adjustable Turn-On Slew Rate
- Minimum Parts Count Solution
- No Charge Pump
- Pb-Free Package Options

Applications

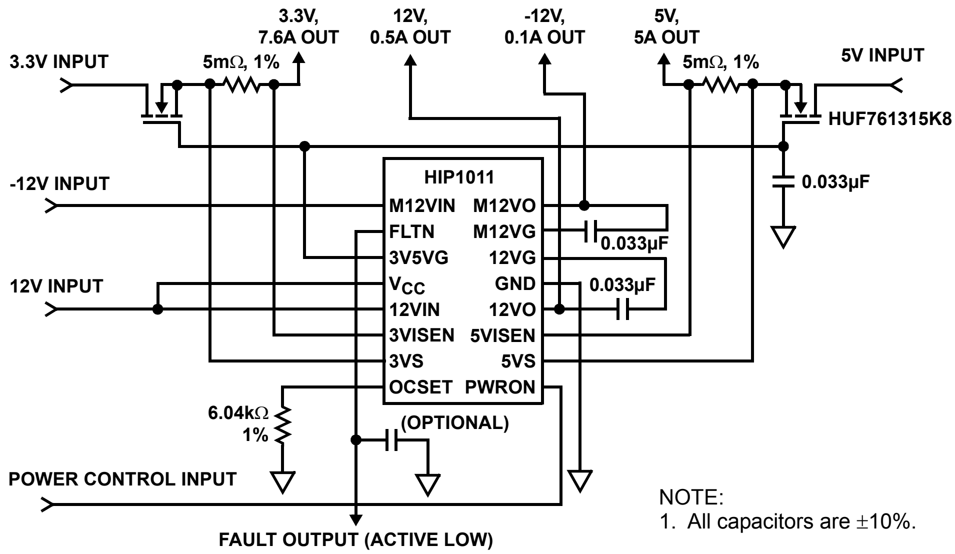
- PCI Hot Plug
- CompactPCI

Pinout

HIP1011
(SOIC)
TOP VIEW

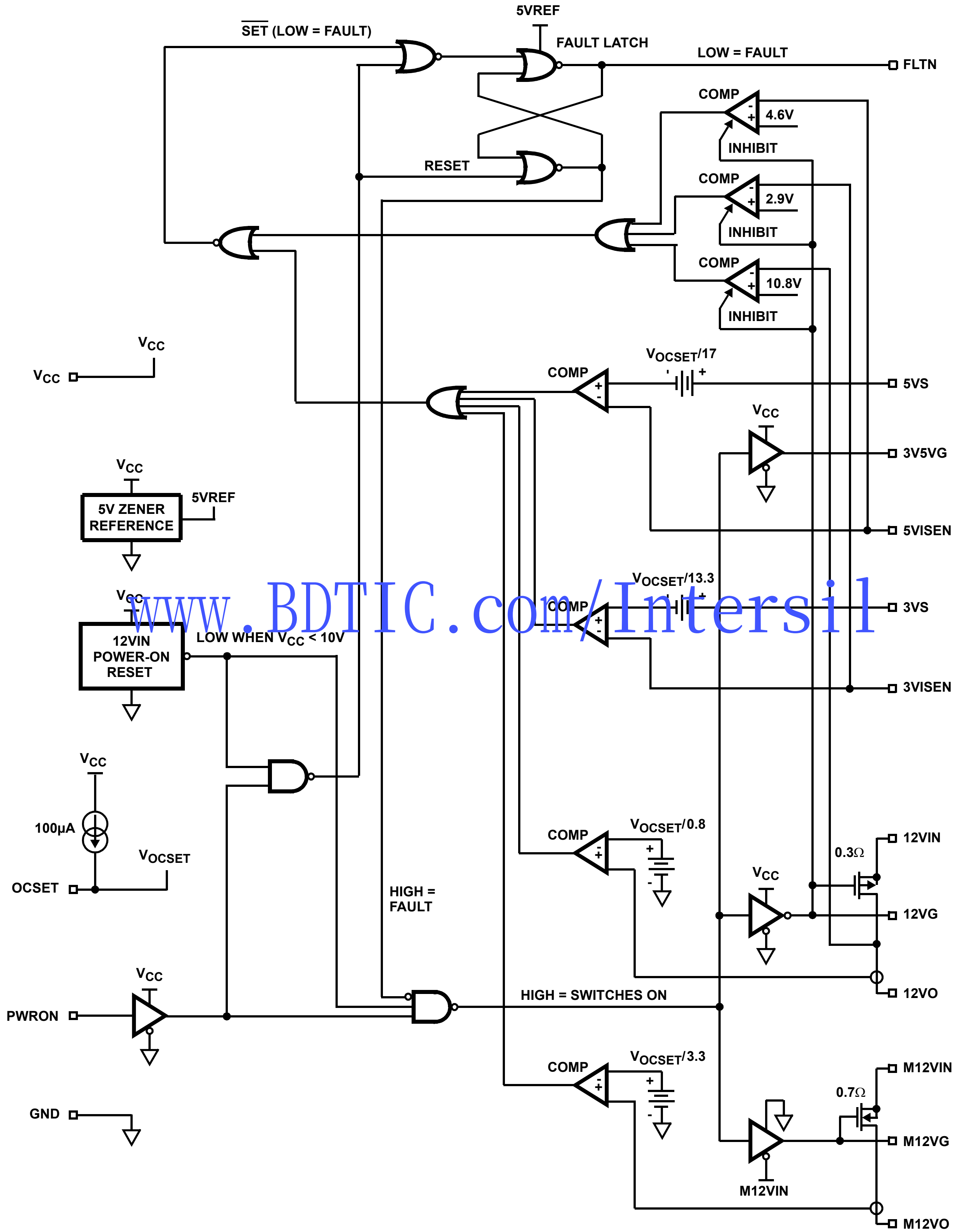


Typical Application



NOTE:
1. All capacitors are ±10%.

Simplified Schematic



Pin Descriptions

PIN	DESIGNATOR	FUNCTION	DESCRIPTION
1	M12VIN	-12V Input	-12V Supply Input. Also provides power to the -12V overcurrent circuitry.
2	FLTN	Fault Output	5V CMOS Fault Output; LOW = FAULT. An optional capacitor may be place from this pin to ground to provide additional immunity from power supply glitches.
3	3V5VG	3.3V/5V Gate Output	Drive the gates of the 3.3V and 5V MOSFETs. Connect a capacitor to ground to set the startup ramp. During turn on, this capacitor is charged with a 25μA current source.
4	VCC	12V V_{CC} Input	Connect to unswitched 12V supply.
5	12VIN	12V Input	Switched 12V supply input.
6	3VISEN	3.3V Current Sense	Connect to the load side of the current sense resistor in series with source of external 3.3V MOSFET.
7	3VS	3.3V Source	Connect to source of 3.3V MOSFET. This connection along with pin 6 (3VISEN) senses the voltage drop across the sense resistor.
8	OCSET	Overcurrent Set	Connect a resistor from this pin to ground to set the overcurrent trip point of all four switches. All four over current trips can be programmed by changing the value of this resistor. The default (6.04kΩ, 1%) is compatible with the maximum allowable currents as outlined in the PCI specification.
9	PWRON	Power On Control	Controls all four switches. High to Turn Switches ON, Low to turn them OFF.
10	5VS	5V Source	Connect to source of 5V MOSFET switch. This connection along with pin 11(5VISEN) senses the voltage drop across the sense resistor.
11	5VISEN	5V Current Sense	Connect to the load side of the current sense resistor in series with source of external 5V MOSFET.
12	12VO	Switched 12V Output	Switched 12V output.
13	GND	Ground	Connect to common of power supplies.
14	12VG	Gate of Internal PMOS	Connect a capacitor between 12VG and 12VO to set the startup ramp for the +12V supply. This capacitor is charged with a 25μA current source during startup. The 3.3V and 5V UV circuitry is enabled after the voltage on 12VG is less than 400mV. Therefore, if the capacitor on the pin 3 (3V5VG) is more than 25% larger than the capacitor on pin 14 (12VG) a false UV may be detected during startup.
15	M12VG	Gate of Internal NMOS	Connect a capacitor between M12VG and M12VO to set the startup ramp for the M12V supply. This capacitor is charged with 25μA during startup.
16	M12VO	Switched -12V Output	Switched 12V Output.

Absolute Maximum Ratings

V_{CC}, 12VIN . . . . -0.5V to +14.0V
12VO . . . . -0.5V to V_{12VIN} +0.5V
12VO, 12VG, 3V5VG . . . . -0.5V to V_{CC} +0.5V
M12VIN . . . . -15.0V to +0.5V
M12VO, M12VG. . . . . V_{M12VIN} -0.5V to +0.5V
3VISEN, 5VISEN . . . . -0.5V to the lesser of V_{CC} or +7.0V
Voltage, Any Other Pin. . . . . -0.5V to +7.0V
12VO Output Current. 3A
M12VO Output Current 0.8A
ESD Classification . . . . 4KeV (HBM)

Operating Conditions

VCC Supply Voltage Range. . . . . +10.8V to +13.2V
±12V, 5V and 3.3V Input Supply Tolerances . . . . ±10%
12VO Output Current. . . . . 0 to +0.5A
M12VO Output Current . . . . 0 to +0.1A
Temperature Range (T_A) . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 68
Maximum Junction Temperature . . . . 125°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

Die Characteristics

Number of Transistors 290

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board in free air. See Technical Brief 379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal 5V and 3.3V Input Supply Voltages, V_{CC} = 12VIN = 12V, M12VIN = -12V, T_A = T_J = 0 to 70°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V/3.3V SUPPLY CONTROL						
5V Overcurrent Threshold	I_{OC5V}	See Figure 1, Typical Application		7.1	-	A
5V Overcurrent Threshold Voltage	V_{OC5V}	V_{OCSET} = 1.2V	66	72	79	mV
5V Undervoltage Trip Threshold	V_{5VUV}		4.42	4.6	4.75	V
5V Undervoltage Fault Response Time	t_{5VUV}		-	150	350	ns
5V Turn-On Time (PWRON High to 5VOUT = 4.75V)		C_{3V5VG} = 0.022µF, C_{5VOUT} = 2000µF, R_L = 1Ω	-	6.5	-	ms
5VS Input Bias Current	IB_{5VS}	PWRON = High	-40	-26	-20	µA
5VISEN Input Bias Current	IB_{5VISEN}	PWRON = High	-160	-140	-110	µA
3V Overcurrent Threshold	I_{OC3V}	See Figure 1, Typical Application	-	9.0	-	A
3V Overcurrent Threshold Voltage	V_{OC3V}	V_{OCSET} = 1.2V	88	95	102	mV
3V Undervoltage Trip Threshold	V_{3VUV}		2.74	2.86	2.97	V
3V Undervoltage Fault Response Time	t_{3VUV}		-	150	350	ns
3V Turn-On Time (PWRON High to 3VOUT = 3.00V)		C_{3V5VG} = 0.022µF, C_{3VOUT} = 2000µF, R_L = 0.43Ω	-	6.5	-	ms
3VS Input Bias Current	IB_{3VS}	PWRON = High	-40	-26	-20	µA
3VISEN Input Bias Current	IB_{3VISEN}	PWRON = High	-160	-140	-110	µA
Gate Output Charge Current	IC_{3V5VG}	PWRON = High, V_{3V5VG} = 2V	22.5	25.0	27.5	µA
Gate Turn-On Time (PWRON High to 3V5VG = 11V)	t_{ON3V5V}	C_{3V5VG} = 0.1µF	-	280	500	µs
Gate Turn-Off Time	$t_{OFF3V5V}$	C_{3V5VG} = 0.1µF, 3V5VG from 9.5 V to 1V	-	13	17	µs
Gate Turn-Off Time		C_{3V5VG} = 0.022µF, 3V5VG Falling 90% to 10%	-	2	-	µs

Electrical Specifications Nominal 5V and 3.3V Input Supply Voltages, V_{CC} = 12VIN = 12V, M12VIN = -12V, T_A = T_J = 0 to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
+12V SUPPLY CONTROL						
On Resistance of Internal PMOS	$r_{DS(ON)12}$	PWRON = High, I_D = 0.5A, T_A = T_J = 25°C	0.18	.300	0.350	Ω
Overcurrent Threshold	I_{OC12V}	V_{OCSET} = 1.2V	1.25	1.50	1.8	A
12V Undervoltage Trip Threshold	V_{12VUV}		10.5	10.8	11.15	V
Undervoltage Fault Response Time	t_{12VUV}		-	150	-	ns
Gate Charge Current	IC_{12VG}	PWRON = High, V_{12VG} = 3V	23.5	25.0	28.5	µA
Turn-On Time (PWRON High to 12VG = 1V)	t_{ON12V}	C_{12VG} = 0.022µF	-	16	20	ms
Turn-Off Time	t_{OFF12V}	C_{12VG} = 0.1µF, 12VG	-	9	12	µs
Turn-Off Time		C_{12VG} = 0.022µF, 12VG Rising 10% - 90%	-	3	-	µs
-12V SUPPLY CONTROL						
On Resistance of Internal NMOS	$r_{DS(ON)M12}$	PWRON = High, I_D = 0.1A, T_A = T_J = 25°C	0.5	0.7	0.9	Ω
Overcurrent Threshold	I_{OCM12V}	V_{OCSET} = 1.2V	0.30	0.37	0.50	A
Gate Output Charge Current	IC_{M12VG}	PWRON = High, V_{M12VG} = -4V	22.5	25	27.5	µA
Turn-On Time (PWRON High to M12VG = -1V)	t_{ONM12V}	C_{M12VG} = 0.022µF	-	160	300	µs
Turn-On Time (PWRON High to M12VO = -10.8V)		C_{M12VG} = 0.022µF, C_{M12VO} = 50µF, R_L = 120Ω	-	16	-	ms
Turn-Off Time	$t_{OFFM12V}$	C_{M12VG} = 0.1µF, M12VG	-	18	23	µs
Turn-Off Time		C_{M12VG} = 0.022µF, M12VG Falling 90% to 10%	-	3	-	µs
M12VIN Input Bias Current	IB_{M12VIN}	PWRON = High	-	2	2.6	mA
CONTROL I/O PINS						
Supply Current	I_{VCC}		4	5	5.8	mA
OCSET Current	I_{OCSET}		95	100	105	µA
Overcurrent Fault Response Time	t_{OC}		-	500	960	ns
PWRON Threshold Voltage	$V_{THPWRON}$		0.8	1.6	2.1	V
FLTN Output Low Voltage	$V_{FLTN,OL}$	I_{FLTN} = 2mA	-	0.6	0.9	V
FLTN Output High Voltage	$V_{FLTN,OH}$	I_{FLTN} = 0 to -4mA	3.9	4.3	4.9	V
FLTN Output Latch Threshold	$V_{FLTN,TH}$		1.8	2.3	3	V
12V Power On Reset Threshold	$V_{POR,TH}$	V_{CC} Voltage Falling	9.4	10	10.6	V

Typical Performance Curves

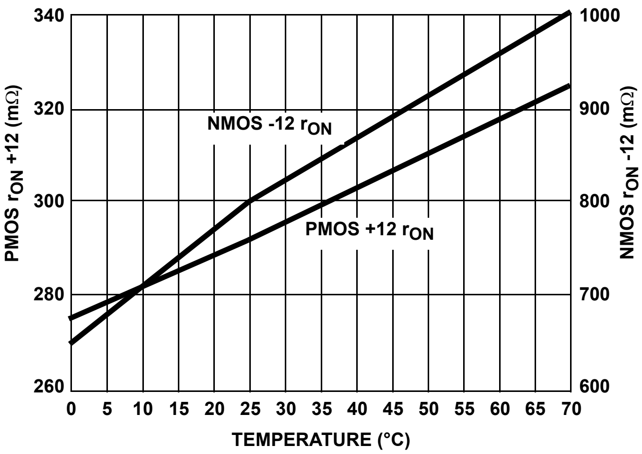


FIGURE 1. r_{ON} vs TEMPERATURE

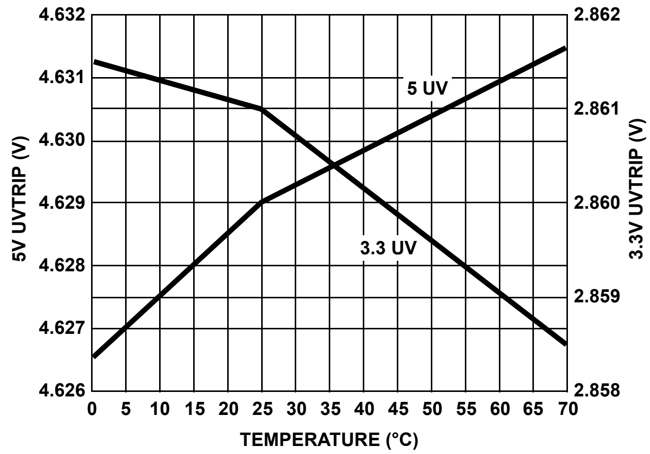
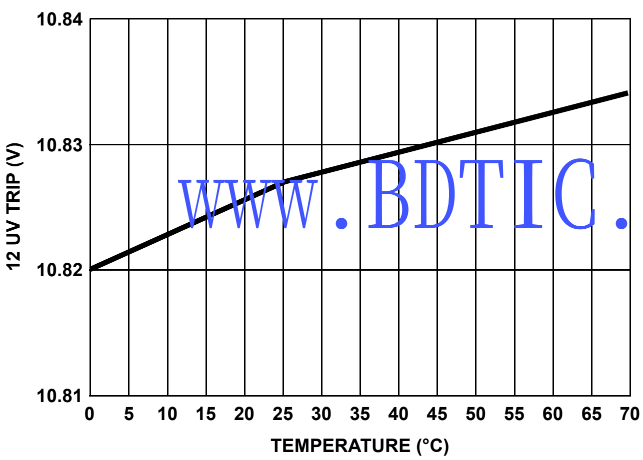


FIGURE 2. UV TRIP vs TEMPERATURE



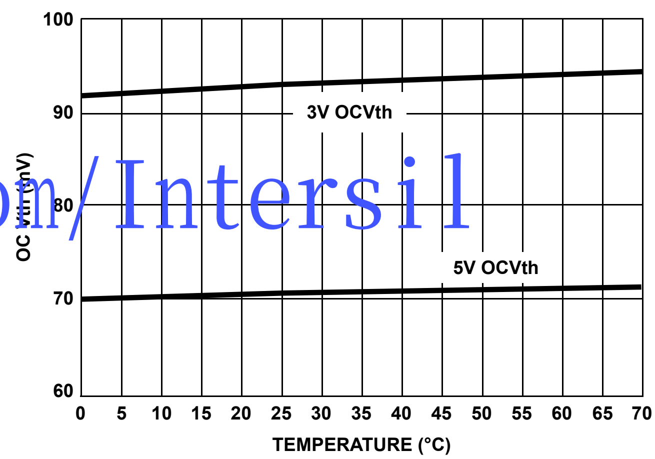


FIGURE 3. 12 UV TRIP vs TEMPERATURE

FIGURE 4. OCVth vs TEMPERATURE (VR_{OCSET} = 1.21V)

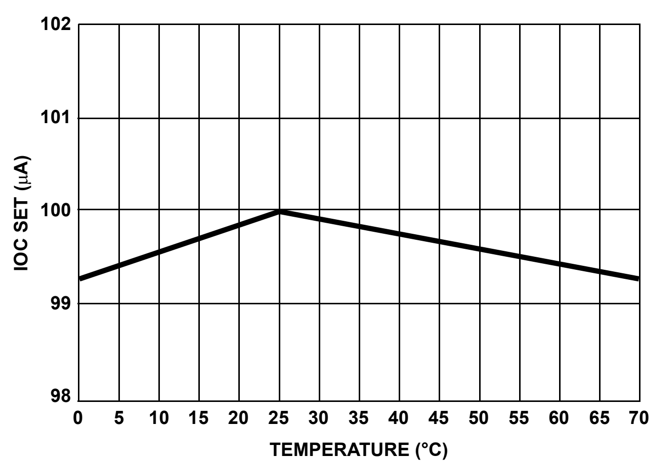
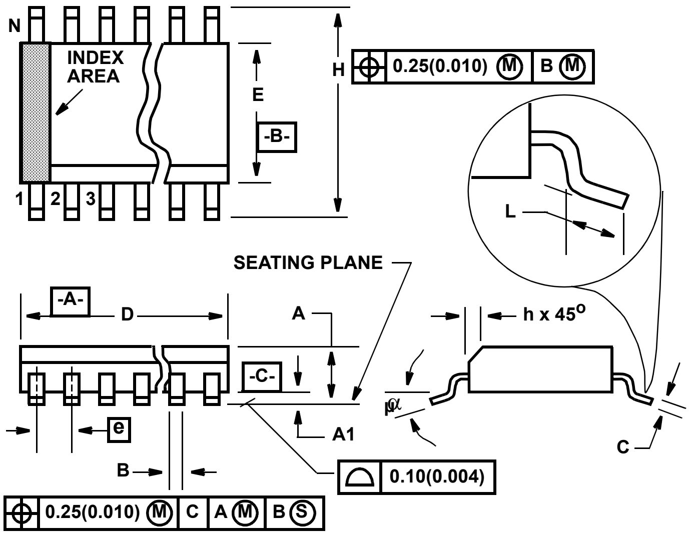


FIGURE 5. OCSET I vs TEMPERATURE

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 02/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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